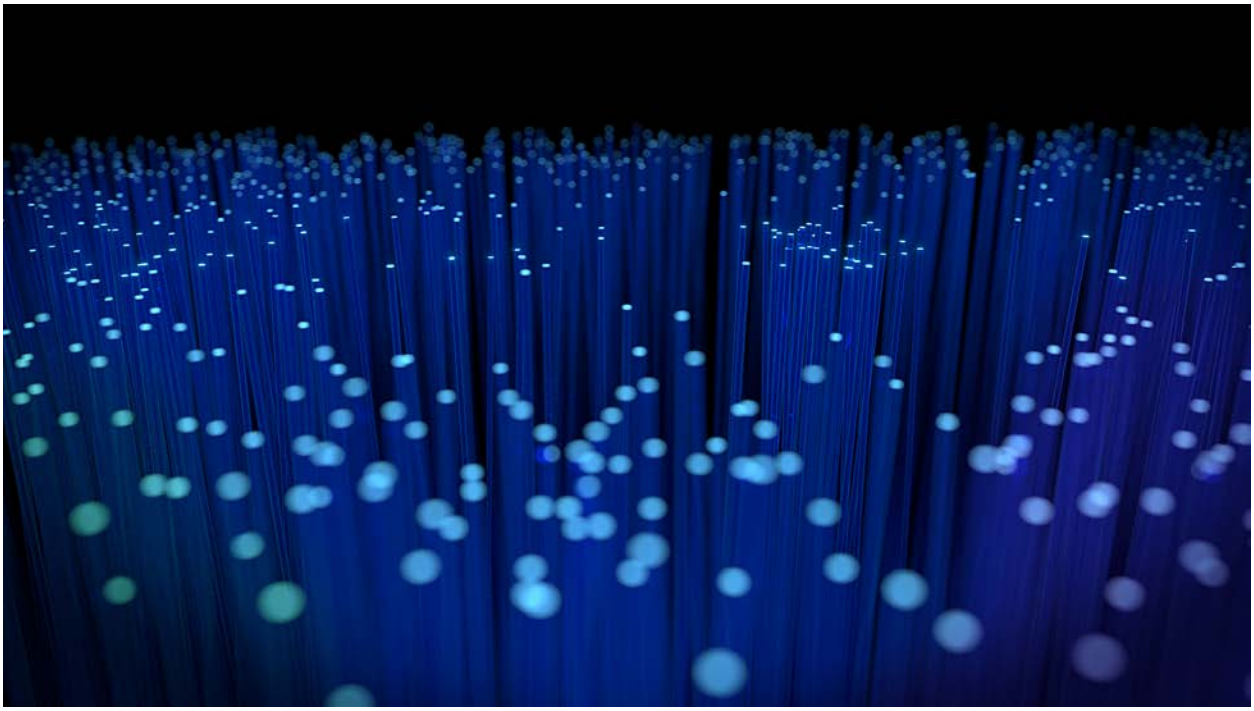
IPSR

Integrated Photonic Systems Roadmap

2016 ROADMAP

EXECUTIVE SUMMARY AND CHAPTER HIGHLIGHTS

DECEMBER 2016



Developed by AIM Photonics Academy

in collaboration with

The MIT Microphotonics Center and the International Electronics Manufacturing Initiative (iNEMI)

AIM Photonics

FOREWORD

The *Integrated Photonic Systems Roadmap* (IPSR) is built on the foundation of the NIST AMTech funded *Photonic Systems Manufacturing Technology Roadmap* (PSMR). It uses the processes and lessons learned from previous roadmap developments by the two Integrated Photonic Systems Roadmap Partners: The International Electronics Manufacturing Initiative and the MIT Microphotonics Center.

In spite of the fact that most companies and individuals are "oversubscribed" in their daily jobs, Seven hundred professionals from 16 countries, representing 254 organizations, came together to create this product. Through sharing, analyzing, debating and reviewing, this diverse team contributed to these initial roadmaps for the photonics industry.

As Principal Investigators of the PSMC Roadmap, we committed to play a major role in the Institutes for Manufacturing Innovation and now in the AIM Photonics Institute to develop a strong integrated photonics manufacturing base.

IPSR SUSTAINABILITY MISSION STATEMENT: The PSMC will become a vital, industry-sustained infrastructure element within the next five years. The IPSR value proposition is based on three pillars: Roadmap, "Big M" Technology Evaluation, and Supply Chain Integration. The pace of value creation is dependent on the emergence of cost effective, platform-based, high volume photonics manufacturing. Significant adoption of integrated photonics manufacturing is required during the next five years for IPSR to meet it sustainability goals.

This completed roadmap includes the "Grand Challenges" that the roadmapping process has identified. We began developing these needs and challenges at the December 7, 2015 PSMC Workshop at MIT where participants developed prioritized lists of gaps for each Technology Working Group. Preliminary lists of the grand challenges provided to AIM Photonics in January 2016 contributed to developing their call for proposals and future R&D projects. At the end of each calendar year we will present the grand challenges, extracted from this roadmap completed under AIM Photonics funding, as prioritized recommendations to AIM Photonics Institute.

We particularly call your attention to the four "Strategic Concerns" described in the Executive Summary. The IPSR has brought commercial elements of the material and technology supply chain to a common table to assess the timelines for volume production of products incorporating integrated photonics. These forums play a critical role in establishing cross-chain technology readiness for an effective manufacturing ecosystem, entry points for SMEs, and teaming opportunities for OEM and user firms. The strategic issues reflect Roadmap TWG Leadership consensus based on participants input, and as projects develop, they should be evaluated frequently by AIM Photonics Institute.

Since December 2015 we have formed five additional Technology Working Groups (TWGs), by splitting two existing TWGs and adding the Electronic-Photonic Design Analysis (EPDA) TWG, the Photonic Sensors TWG and the Workforce Developent and Education TWG. We have added three new Product Sector Emulator Groups (PEGs), Automotive, Photonic Sensors, and RF Photonics.

We welcome your thoughts and comments as you use this important reference document in your planning processes.

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EXECUTIVE SUMMARY

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EXECUTIVE SUMMARY

SITUATION ANALYSIS

MARKET

The boundaries among computers, communications, and entertainment products have blurred. Flat panel displays are the norm for virtually all applications, with touch screen technology becoming dominant in a number of product categories. Wireless products continue to proliferate, and this advance is opening up new applications in a number of segments. We are seeing dramatic growth of mobile Internet applications, including the massive demands for mobile data, the growth of mobile video, and the dramatic increase of smart phones as the gateway to the web.

According to a June 2016 report from Cisco Systems. Annual global IP traffic will surpass the zettabyte (1 ZB = 1000 exabytes [EB]) threshold in 2016. Global IP traffic will reach 1.1 ZB per year or 88.7 EB (one billion gigabytes [GB]) per month in 2016. By 2020, global IP traffic will reach 2.3 ZB per year, or 194 EB per month. Global IP traffic will increase nearly threefold over the next 5 years, and will have increased nearly 100-fold from 2005 to 2020. Overall, IP traffic will grow at a compound annual growth rate (CAGR) of 22 percent from 2015 to 2020.

End users desire more integrated, 'open-source' data center systems, and the end users have emerged as a powerful factor in data center hardware selection. Consequently, the center of power has shifted from original equipment manufacturers (OEMs) to the large end users. End users are establishing specifications for cost, energy, and bandwidth density. To reach their performance goals they are evaluating the impact of disaggregation, virtualization, direct memory access, and microservers.

Today integrated optics technology is proprietary and is not manufactured in high volume. Having multiple supply chain sources is difficult. Establishing an enabling silicon photonics technology as envisioned in this roadmap is a necessary step to achieving low-cost, high-volume manufacturing in this rapidly expanding market.

The Internet of Things (IoT) ecosystem is hard to define, complex, and difficult to capture due to the vast number of possibilities and the rapidity with which it is expanding. The technologies enabling this growth are being developed faster than new market opportunities can be identified. Two key technologies for this market are (1) improvments in low-power, high-speed communications and (2) new sensors. Technologies that integrate photonics systems are well positioned to address new market opportunities. The success of IoT depends strongly on standardization which provides interoperability, compatibility, reliability, higher manufacturing volumes, and effective operations on a global scale.

The Automotive Product Emulator, the first of three new IPSR emulators, identifies the automotive application needs that may be met best with Integrated Photonics. The integrated photonic systems applications considered in this emulator are:

1. Advanced Driver Assistance Systems (ADAS) utilizing integrated photonic technology in Light Detection and Ranging (LIDAR) systems. Lidar[1] is a remote sensing method that uses light to measure range.
2. Photonic Sensors for a wide range of applications. and
3. Optical Local Area Networks (LAN).

The great uncertainty in this product sector is the rate of development and application of low-cost lidar and integrated photonic sensors for ADAS. The enabling technology and specifications differ for various systems and will change over time. Some of today's systems like Tesla's do not even use lidar. Nevertheless, most systems use multiple sensors and proprietary algorithms to integrate visual, RF, and IR information. The rapidly changing market in the Automotive Sector needs increased examination in future Integrated Photonic Systems Roadmaps.

The Photonic Sensors Product Emulator addresses integrated electronic-photonic technology applications for sensors. There are a number of sensor applications that could be met with integrated photonic technology, but there are also competing technologies, such as micro electronic mechanical systems (MEMS), that could meet the current application needs. This PEG addresses the sensors needs, but not the technology solutions that are addressed in the Photonic Sensors TWG. The objective of this TWG is to identify markets that might be early adopters of integrated photonic systems technology

The RF Photonics Product Emulator covers integrated electronic-photonic technology applications that have been identified by AIM Photonics to be particularly important to meet high-speed analog communication needs over optical fibers. Electronic-photonic integration not only makes use of existing Complementary Metal-Oxide Semiconductor (CMOS) manufacturing infrastructure, to produce low-cost analog or digital components, but also seeks to benefit from a close interaction between a controlling electronics layer and an integrated photonic circuit to increase the functionality and performance of the system over the current state-of-the-art (SoA).

TECHNOLOGY

Cisco Systems projects that Globally, IP video traffic will be 82 percent of all consumer Internet traffic by 2020, up from 70 percent in 2015. Global IP video traffic is projected to grow threefold from 2015 to 2020, a CAGR of 26 percent. Internet video traffic is anticipated to grow fourfold from 2015 to 2020, a CAGR of 31 percent. The telecommunications system and everything down to semiconductor chips must grow proportionally in both capacity and performance to support this traffic increase. In addition, new mobile applications require large amounts of computing power resulting in warehouse computers that consume 50+ megawatts. These changes drive optical technologies. As these data rates increase, optical methods are replacing copper/electronic methods at ever shorter distances. The current transition point is at data rates of 10 Gb/s and distances of 1 to 10 meters. When data rates or distances greater than those are needed, optical methods are attractive because they often reduce both power consumption and physical size up to 75%.

[1] As with radar, we will use lower case "lidar" throughput the remainder of the chapter.

Global network requirements are changing with the rise of the IoT and the migration of data, logic, and applications to the cloud. High-density 3D packaging of complete functional blocks has become the major technology challenge. These changing requirements must be accommodated while maintaining the pace of progress in size, cost, and power per function that we have enjoyed for the past 50 years, based primarily on the benefits of Moore's Law scaling of CMOS electronics. The introduction of photonics into the transmission, processing, and even generation of data through optically based technologies is a key enabling factor for continued progress as the benefits derived from Moore's Law scaling begin to slow.

HIGHLIGHTED NEEDS

During the 15-year life of this roadmap we must change the global network, the components in it and most of the elements attached to it, in order to meet market needs including:

- 10^4 improvement in power efficiency,
- 10^4 improvement in cost per function, and
- 10^6 improvement in the number of network ports.

All of these improvements are needed at no increase in total cost!

The potential sources of improvement include:

1. Disaggregation to improve the utilization of microprocessors from 15% to close to 100% (5X improvement);
2. Microservers to replace blade servers (10X improvement);
3. Direct memory access vs going through internet protocols in data centers (10X improvement);
4. Broad implementation of circuit switching and switching in the optical domain (10X improvement); and
5. Further improvement in devices i.e. More Moore meaning CMOS at 10 nm nodes (5X improvement).

Optical methods that reduce power and increase data density will be used widely to implement these improvements.

More importantly, achieving this challenging task will require strengthening the mechanisms for cooperation among industries and among researchers who are all working in advanced technologies. Cooperation among OEMs, Original Design Manufacturers (ODMs), EMS, and component suppliers needs to focus on the right technology and to find a way to deploy it in a timely manner. A first step to achieving this cooperation in the supply chain was the discussion stimulated among 700 stakeholders at all levels of the research, development, and manufacturing supply chain in preparing this roadmap.

As noted in the introduction to this roadmap, the key activities of IPSR since May 2014 have focused upon (1) building mutual trust and cooperation among the supply chain stakeholders in order to establish common visions for high-volume photonic system manufacturing and for the

technology gaps that need to be closed and (2) developing a cohesive roadmap for integrated photonic system design.

The need for disruptive technologies to meet these challenges provides opportunities for innovation. In order to ensure success, the supply chain must be willing to invest with a long-term perspective in mind. The 2016 Roadmap has identified significant needs in a number of areas as highlighted in the following sections of this Executive Summary: Standards Development, Design Technologies, Training Designers, Manufacturing Technologies, Materials, Component Technology, and Security and Information Management.

STANDARDS DEVELOPMENT

A number of areas addressed in the roadmap identified the need for standards development. Many roadmap participants believe that the lack of timely standards is slowing significantly both the implementation of technology and the growth of markets. Several consortia such as the Consortium for On-Board Optics (COBO) are working to create industry standards that will allow:

- Interoperability,
- Interchangeability, and
- Broader market potential.

With the need for standards acknowledged, note that standards generally emerge as the industry learns that they offer value and then adopts them. Generally some higher level of industry does not impose standards.

DESIGN TECHNOLOGIES

Design and simulation tools — or the lack of these capabilities — can delay the rapid introduction of new technologies and market growth. Particular areas where capabilities need to improve include:

- Modeling, Simulation, and Design tools for Integrated Photonic Systems;
- Design software able to utilize Hooke's General Law as a function of temperature;
- Reliability, mechanical analysis, and simulations;
  - Interfacial delamination,
  - Moisture modeling,
  - Material characterization, and
  - Process modeling;
- Prediction of lifetime based on physics of failure;
- Thermal and thermo-fluid simulations;
  - Passive thermal management,
  - Efficient and accurate thermal radiation, and

- Increased need for system level simulations.

During 2016 IPSR established an Electronic-Photonic Design Automation TWG to identify and prioritize the needs for design and simulation tools. Their first output appears in this roadmap.

TRAINING DESIGNERS

Low cost, high-performance optical products begin with good design. To use this enabling technology effectively requires that designers understand the technology and both manufacturing capabilities and limitations. Important factors that designers need to understand include:

- Design for Manufacturing, Test, and Cost;
- Minimizing the number of parts;
- Choosing parts that are adequate but not overly specified;
- Minimizing the number of assembly steps;
- Understanding details of parts and working with manufacturers to ensure that parts will have;
    - The necessary dimensional consistency,
    - Suitable location reference points,
    - Surfaces to which suitable joints can be made, and
    - Shipping package containers that interface with manufacturing assembly equipment;
- Evaluating the extremes of part specifications and dimensional tolerances to ensure robust design;
- Maximizing the tolerances required as best as possible; and
- Ensuring that dimensional requirements can be achieved.

In 2017 the Aim Photonics Academy will introduce programs to address these needs.

MANUFACTURING TECHNOLOGIES

Since research and development (R&D) responsibility is shifting from OEMs to ODMs and EMS companies, government, academia, and industry consortia need to formulate new ways to adopt and develop emerging technologies into needed manufacturing processes. These new approaches will have to be consistent with viable business models and the avalibility of funding in order to create new industrial infrastructures. Specific manufacturing development targets include:

- Integrated photonics for high-volume applications,
- Process development to accelerate miniaturization,
- Assembly processes that support 3D structures and low-temperature processing,
- Cost-effective product traceability solutions,
- Anti-counterfeiting solutions,

- Reliability methodologies for manufacturing 3D structures,
- Extension of electronic manufacturing processes to address photonics, and
- Inspection/test technologies to keep up with increasing density of component packages.

MATERIALS

Meeting the increased performance requirements of silicon integrated photonics will require development of new materials with a variety of different properties. Data sheets for electronic materials need to be expanded to include optical properties. Ensuring the reliability of these materials during the life of the product will be one of the gating issues for market introduction.

COMPONENT TECHNOLOGY

A standard approach to package- and board-level interconnection is required to achieve low-cost components including:

- Printed wiring boards with embedded waveguides,
- Embedded waveguide-to-surface layer connectors,
- Surface mount interposers and sockets,
- Surface mount optical transceivers $\geq$ 100-400Gbps, and
- Direct chip-attach optical interconnect.

The IPSR leadership team has established a board-level optical interconnection effort to form short-term industrial consortia to address three of these needs. The first phase project is to design, assemble, and test demonstration prototypes of board-level interconnect systems based on single-mode (SM) optical fiber, expanded-beam optical coupling, and silicon photonics transceivers. The effort will be self-funded by the participants.

SECURITY AND INFORMATION MANAGEMENT

Trusted foundries for military applications and component traceability, security, and anti-counterfeiting protection for all applications are issues that must be addressed as new enabling technology is introduced. Information management and security is a major concern for the IoT, sensors, and ADAS.

PARADIGM SHIFTS

The predominant paradigm shift identified in this Roadmap is the impact of cloud-connected digital devices. The movement to the cloud has the potential to cause major disruptions across the electronics and photonics industries. In the next few years, the industry is likely to see major transitions in business models. We expect to see more of the following:

- Huge data centers operating more like utilities (selling data services),
- Local compute and storage growth may slow (as data moves to the cloud), and
- “Rent vs. buy” for software; i.e., monthly usage fee for cloud-based solutions.

Other paradigm shifts identified in the IPSR Roadmap include:

- The need to continuously introduce complex multifunctional products to address converging markets favors the use of modular components or SiP (2D, 2.5D & 3D);
- The IoT is making sensors ubiquitous; however, there are concerns about network security as cyber attacks become more pervasive;
- The rapid introduction of ADAS into automotive products with no consensus on the winning, low-cost technology that provides the necessary safety; and
- The disruptive technology required to produce a 1,000-fold improvement in data-center performance at constant cost.

STRATEGIC CONCERNS

- ***Acquiring support to reduce the risk of introducing needed paradigm changing technologies into volume production***: Several National Research Council Reports on the introduction of new enabling manufacturing technology have demonstrated that current American business models discourage key suppliers of enabling technology products from making the necessary R&D and capital investment needed for success. One of many examples is the failure to develop flat panel display technology in the United States. This concern has been one key reason for establishing the National Network for Manufacturing Innovation (NNMIs). The development of this roadmap has revealed a specific concern that American manufacturers of enabling components may need support to develop the necessary electronic-photonic packaging, substrates, and connectors in a timely manner to meet the needs identified in this roadmap. We anticipate that this need will most likely remain in future editions of the roadmap.
- ***Copper vs. Fiber***: Copper-based circuitry has advanced well beyond earlier capabilities and will continue to advance toward 100 GB throughput for short ~1m distances. There are companies working diligently on optical fiber solutions, but there are fewer than ten companies doing this in the connector and PCB industries. There are many more companies making cable assemblies. At the core of optical fiber is one major US Company, Corning Inc.
- ***Industry Cooperation:*** Obtaining cooperation from industry personnel is difficult because of perceived intellectual property issues involving their customers. However, the IPSR Board-Level Optical Interconnect Consortium is demonstrating that it can be achieved.
- ***Cost Targets:*** Proposed cost targets in an established industry are viewed as unrealistic unless standards are developed to commoditize the components.

KEY RECOMMENDATIONS

ROADMAPPING

We are adding additional Technology Working Groups (TWGs) and Product Emulator Groups (PEGs) to address needs identified by AIM Photonics. We began this process with the formation of an Electronic-Photonic Design Automation (EPDA) TWG and a Photonic Sensors TWG. We have identified a need for greater integration between the IPRS Roadmapping Process and the AIM Photonic Technical Planning Process so that AIM Photonics can develop the key enabling technologies in time to meet the growing market needs for integrated photonics.

DESIGN

There are two major recommendations for photonic design:

1. Develop college- and graduate-level education programs to educate students to design integrated photonic systems and courses to retrain electronic designers.
2. Develop integrated design tools.

The first need is being defined further in the new IPSR Workforce Development and Education TWG.

The increasing end user and OEM focus on time-to-market and the complexity of emerging technology requires significant development and investment in design tool infrastructure. The following areas call for increased research and development:

- Reliability, mechanical analysis and simulations including
    - Material characterization including optical properties,
    - Interfacial delamination and chip-package interaction (CPI),
    - Process modeling,
    - Environmental stress modeling and,
        - Moisture,
        - Temperature cycling,
        - Shock,
        - Etc.,
    - Joint reliability modeling;
- Research and development of thermal and thermo-fluid simulations;
- Tools and methodology research and development in the manufacturing systems/supply chain management areas;
- Projected development and research for simulations in emerging areas; e.g., photonics, nano devices and materials;
- Co-design of optical, mechanical, thermal, and electrical performance of the entire chip, package, and associated heat removal structures; and
- New capability to close the gap between chip and substrate interconnect density.

MANUFACTURING TECHNOLOGY

Four strategic needs have emerged for Manufacturing Technology:

1. Miniaturization of the product,
2. Simplified, next-generation assembly processes,
3. Increased accuracy for assembling optical components, and
4. Fewer components to assemble.

These strategic needs generate the following recommendations in manufacturing technology:

- New approaches to organic substrate manufacturing that provide dramatic increases in density, reduced process variability, improved electrical performance and significant cost reduction;
- Manufacturing processes at all packaging levels to deal with warpage and thin-format products;
- 3D package stacking development with emphasis on
    - Assembly,
    - Testing,
    - Cooling, and
    - Reliability;
- There are compelling advantages of 3D through silicon via (TSV) technology; however, commercialization is gated by the development of the industry infrastructure and the supply chain;
- Low-temperature assembly; and
- Self-aligning assembly and stress-free joining technology for photonic components.

MATERIALS DEVELOPMENT

The need for materials development that addresses the following findings is clear:

- A combination of materials and fabrication research is needed to support the development of monolithically integrated optics and electronics that take advantage of the electronics infrastructure;
- Low-cost, higher thermal conducting packaging materials, such as adhesives, thermal pastes and thermal heat spreaders;
- New interconnect technologies deploying nano-materials to support decreased pitch and increased interconnect frequencies;
- High-performance laminates that are competitively priced;
- Clearer specifications for new materials that are supported by a broad base of customers, to increase market size and reduce the risk for materials R&D; and
- Reliability testing methodologies for new materials.

INTRODUCTION TO CHAPTER HIGHLIGHTS

A list of key roadmap drivers was developed for the product sectors, known as PEGs.

The TWGs use the projected technology needs from PEGs as input for the TWG Roadmaps. If the global photonics-electronics infrastructure can meet or exceed the key Product Sector drivers, through implementation of the strategies discussed in the IPSR TWG Roadmaps, then the industry can enable faster technology deployment and increased growth in global market for electronic products. The focus of IPSR's implementation activities is to identify gaps and issues that would prevent us from attaining these key parameters. IPSR will then support AIM Photonics in developing a five-year technology plan that proposes projects to address prioritized gaps.

Because of the broad coverage of these roadmaps, many acronyms from diverse fields appear in the text. For reading convenience, an effort has been made to define an acronym the first time that it is used in a chapter and for refrence/convinecne all acronyms have been listed in a section on their own.

PRODUCT EMULATOR GROUPS

DATA CENTER PRODUCT SECTOR

The Data Center Product Sector Emulator covers the technologies that enable high-performance computing systems, data centers, and communications systems. The data explosion generated by the growth in social networks and digital entertainment, cloud computing, and the Internet of Things (IoT) are driving radical growth of data centers and the need for high-bandwidth, low-latency communications.

These forces are transforming the data-center structures to a higher level of integration for computing, storage and networking components. The data bandwidth demand is resulting in systems with ever faster interconnect speeds, even as processor speed remains constant. The size of the data centers creates a challenge for power demand, creating an increasing focus on power efficiency. The data centers have an increasing number of systems residing in an environment of higher temperature, humidity and corrosive elements to reduce the operation costs and manage the total cost of ownership of these systems. Achieving this rapid growth places increasing demands on increasing the performance and decreasing the cost of next-generation equipment. Because of the capital requirements for adding capacity, all segments are undergoing rapid consolidation and movement to external cloud services.

The industry analysis by IHS Markit (IHS) projects a factory OEM revenue growth of 4.4% CAGR during the next ten years from a cumulative $162B today to $273B in 2025. The growth in the Data Center sector is particularly strong, growing from $7B today to $22B in 2025 driven by the rapid increase in data traffic. The rate of innovation in the Data Center sector is high, enabled in part by the open-source concepts of hardware and software. The Enterprise Communications sector is still recovering from the economic meltdown of 2008-2009 and upgrades are slow. However, metro networks are heavily utilized, with the proliferation of 4G and investments including 100G

interconnect. Service Provider Equipment is tied more closely to short-term economic trends and forecasts of growth. Technology upgrades and convergence is driving growth of 5.4% CAGR.

The assembly and packaging technology to support the data centers continues to advance. In particular the need for high-speed, low-latency data transfer is driving the need for integrated silicon photonic components. The enabling technologies include:

- Heterogeneous packaging including TSVs for stacked chips and silicon interposers,
- System in Package (SiP) and Package on Package (PoP),
- Integrated silicon photonics systems,
- Lower loss interconnects including low-loss laminates in printed circuit boards and packages,
- More efficient power conversion e.g. wide band-gap materials.

The Data Center Emulator focuses on enumerating the trends during the next decade that integrated electronics components and technology must meet for the Data Center Market. These particular trends focus on:

- Packaging technology and costs,
- PCB and connector technologies and costs, and
- Testing and assembly/joining technologies.

INTERNET OF THINGS (IOT) PRODUCT SECTOR

International initiatives like The International Year of Light (IYL) 2015, the National Photonics Initiative (NPI), Horizon 2020, the Brain Research through Advancing Innovative Neurotechnologies (BRAIN) initiative, and the Integrated Photonics Institute for Manufacturing Innovation (IP-IMI) can only help reinforce what our industry already knows: Photonics plays a significant role in our daily lives and will only become more prevalent as future applications emerge.

The impact of the IoT on daily life is expected to be as great as the impact of the Internet over the last two decades. Thus, the IoT is recognized as “the next phase of Internet.” Enabling technologies include sensors and actuators, photonics, Wireless Sensor Networks (WSN), Intelligent and Interactive Packaging (I2Pack), real-time embedded systems, Micro Electro-Mechanical Systems (MEMS), mobile internet access, cloud computing, Radio Frequency ID (RFID), Machine-to-Machine (M2M) communication, Human Machine Interaction (HMI), middleware, Service Oriented Architecture (SOA), Enterprise Information Systems (EIS), data mining, etc. The IoT has thus become a new paradigm of the evolution of information and communication technology.

The IoT is expected to change and evolve continually – rapidly! There are already more smart devices and electronic gadgets on earth than people! According to the IDC, the digital universe will reach 44 trillion gigabytes of data by 2020 from a variety of “things,” such as medical implants, wearable technology, and even vending machines. Today, according to CloudTweaks, more than 2.5 billion gigabytes of data are generated every day. More devices are being added on

a daily basis and the industry is still in its infancy. The IoT taps into data that allows us to make more informed decisions, faster. Many of the challenges facing the industry are yet unknown: Unknown devices. Unknown applications. Unknown use cases. Given this reality, there needs to be flexibility in all facets of development. Processors and microcontrollers that range from 16–1500 MHz to address the full spectrum of applications from a Microcontroller Unit (MCU) in a small, energy-harvested wireless sensor node to high-performance, multi-core processors for IoT infrastructure. A wide variety of wired, wireless and photonic connectivity technologies are required to meet the various needs of the market. A wide selection of sensors, mixed-signal and power-management technologies are desired to provide the user interface to the IoT and energy-friendly designs.

The new technologies that are becoming available must meet these challenges–-complexity, connectivity, security, bandwidth, power, and environmental. Key, new processor packaging technologies are being developed with some fundamental changes in the rest of the electronics industry and how it impacts the technology that can be leveraged. With the IoT, a new set of technologies will evolve, but often at a much different scale of size, bandwidth and latency than required by typical data centers.

AUTOMOTIVE PRODUCT SECTOR

The Automotive Sector potentially can become the fastest growing sector for low-cost integrated photonic systems. The IPSR Automotive Product Emulator identifies those automotive application needs that may be met most successfully with Integrated Photonics. The integrated photonic systems applications considered in this emulator are:

- Advanced Driver Assistance Systems (ADAS) utilizing integrated photonic technology in Light Detection and Ranging (LIDAR) systems. Lidar is a remote sensing method that uses light in the form of a pulsed laser to measure ranges;
- Photonic Sensors for a wide range of applications; and
- Optical Local Area Networks (OLAN).

The two main factors that distinguish the Automotive Product Sector Emulator from the other IPSR Product Emulators are:

- The environment in which the product must perform, and
- The possibility of disruptive technology change to electric power and ADAS.

The automotive electronics industry accounted for revenue of $107B in 2013. The sector is still expected to experience relatively strong growth through 2025, increasing at a CAAGR of about almost 4.4% per year. Most experts anticipate that ADAS will require numerous sensors and low-cost lidar. The confluence of accelerating electronic content across the globe with strong emerging market vehicle sales growth bodes well for the automotive electronics market during the next six years.

From a low of more than 60M vehicles produced in 2009 during the recession, global passenger car and light commercial vehicle unit shipments rebounded to more than 75M in 2011. China has surpassed the U.S. as the largest car market in the world. Overall vehicle unit shipment growth off the 2011 base is expected to grow by just under 6% per year thereafter.

The main factor that distinguishes the Automotive Product Sector Emulator from the other IPSR Product Sectors is the environment in which the product must perform. The products must perform reliably in automobiles, light-duty, medium-duty, and heavy-duty trucks. Many of the attributes, such as cost, density, and components, overlap into the other sectors. Increasing density is important for these applications because of cost, size, and weight reductions. The assembly and manufacturing requirements are also critical to achieve/maintain reliability which inturn mandates that rigorous testing is performed. Automotive applications are extremely cost sensitive and therefore require cost targets similar to those found in a Consumer Product Emulator. Increasing density is important for these applications because of cost, size, and weight reductions. The assembly and manufacturing associated with handset equipment imposes critical requirements again due to reliability. The challenge for the automotive product sector is to adapt other sectors' technologies to meet the high-temperature, environmental, and reliability requirements — all at low cost.

The great uncertainty in this product sector is the rate of development and application of low-cost Integrated Photonic Circuit (IPC)-based lidar and integrated photonic sensors for ADAS. In the last twelve months we have seen major announcements on new "low cost" lidar systems, but what is low cost? Velodyne sells rotating lidar systems reportedly used by Baidu, Ford, Google, Nissan, and Volvo in their autonomous test vehicles. The price of the Velodyne HDL-64E used in the Google car is about $80,000; Delphi and their partner Quanergy are working towards a $250 lidar with automobile-grade connectors. But as we will show in the section on ADAS and lidar, we are not necessarily comparing apples with apples. The enabling technology and specifications differ for various systems. Some systems like the ones currently in use by Tesla do not use lidar. Most systems use multiple sensors and proprietary algorithms to integrate the visual, RF, and IR information. The rapidly changing market in the automotive sector needs increased examination in future Integrated Photonic Systems Roadmaps.

PHOTONIC SENSORS PRODUCT SECTOR

The IPSR Sensors Product Sector addresses integrated electronic-photonic technology applications for sensors. There are a number of sensor applications that could be met with integrated photonic technology, but there are also competing technologies, such as MEMS that could meet the current application needs. This PEG addresses the sensors needs, but not the technology solutions that are addressed in the Photonic Sensors TWG. The objective of this TWG is to identify markets that might be early adopters of integrated photonic systems technology.

The motivations for electronic-photonic integration are (1) to utilize the existing CMOS manufacturing investment to produce low-cost analog or digital components and (2) to increase the functionality and performance by augmenting electronics solutions with photonic technologies. These enabling technologies include:

- Heterogeneous packaging TSVs for stacked chips and silicon interposers,
- SiP and PoP,
- Integrated silicon photonics systems,
- Lower loss interconnects (low-loss laminates in printed circuit boards and packages), and

- More efficient power conversion (e.g. wide band-gap materials).

The Sensor Emulator focuses on enumerating the trends during the next decade that integrated electronics-photonics technology must meet for the Sensor Market. These particular trends focus on:

- Packaging technology,
- PCB and connector technologies and costs, and
- Testing and assembly/joining technologies

RF PHOTONICS PRODUCT SECTOR

The RF Photonics Product Sector Emulator covers the integrated electronic-photonic technology applications that have been identified by AIM Photonics to be particularly important to meet high-speed analog communication needs over optical fiber links. The reason for electronic-photonic integration is to utilize the existing CMOS manufacturing investment to produce low-cost analog or digital components and to increase the functionality and performance with photonic technology. The benefits of using photonic technology are:

- Reduced Size, Weight, and Power (SWaP),
- Improved performance,
- Reduced number of optical and/or electrical interfaces,
- Realization of new functionalities,
- Reduced cost for volume manufacturing, and
- Increased reliability (vs. discrete solutions).

In particular the need for high-speed, low-latency is driving the need for integrated silicon photonic components. The enabling technologies include:

- Heterogeneous packaging TSVs for stacked chips and silicon interposers,
- SiP and PoP,
- Integrated silicon photonics systems,
- Lower loss interconnects (low-loss laminates in printed circuit boards and packages), and
- More efficient power conversion (e.g. wide band-gap materials).

The RF Photonics Product Sector focuses on the trends that will be critical during the next decade:

- Component development,
- Packaging technology, and
- PCB and connector technology and costs, testing and assembly/joining technologies.

COST EMULATORS

The goal of the IPSR roadmapping effort is to identify the opportunities, obstacles, and potential solutions to realizing broad adoption of photonics in a range of applications. In doing so, the industry will have the opportunity to coordinate resources and overcome those obstacles more

efficiently. With a technology that is evolving rapidly, many potential solutions will be proposed to realize the future photonics vision. Each of those potential solutions will need to be vetted not only to ensure that they will provide adequate performance (e.g. with respect to speed and size), but also for their potential economic ramifications. It will be important to target industry resources within the portfolio of solutions that promise both the best technical and economic performance.

To address the latter part of this challenge, the IPSR roadmap is in the process of developing a generalized cost-modeling tool that can be applied to bind the cost implications of proposed solutions. The goal of such a tool can be simply stated: to quantify the cost implications of proposed process flows. Such information should allow the roadmapping teams to focus their resources more rapidly and earlier in the technology development process. Currently, the IPSR cost modeling tool focuses on the costs of packaging and assembly. The long-term goal is to expand its scope to encompass all relevant production related costs. The cost emulator chapter delves into the motivation for creating such a tool and then describes the current state of the IPSR tool primarily through a case example of optical transceivers.

We have limited our first analysis to the packaging of the optical devices into a module. The costs of components are taken as inputs rather than calculating them directly. Although we carry out sensitivities to understand the potential implications of various levels of component costs, the reader should view this analysis as incomplete. Although incomplete, this analysis serves to demonstrate the potential for detail process-based cost analysis to address critical photonics questions.

Preliminary results suggest that:

- Monolithic integration of the Datacom transceiver has the potential to significantly lower packaging cost for both high- and low-volume production;
- The key cost savings opportunity for integrating in the near term derives from avoiding the expense of assembling and packaging the interposer layer; and
- Integration has significant cost advantages even if optical chip yields were to fall well below the modeled “baseline” values.

TECHNOLOGY WORKING GROUPS

The Technology Working Group (TWG) Chapters in this roadmap are:

- Monolithic Integration TWG
- Packaging of Electronic Photonic Systems TWG
- Connectors TWG
- Substrate TWG
- Assembly TWG
- Test TWG
- Photonic Sensors TWG
- Electronic Photonic Design Automation TWG
- Education & Workforce Development TWG

MONOLITHIC INTEGRATION

The advent of cloud computing, supercomputers and short data center product cycles have created additional demand for board and I/O-level photonic components and subsystems, including rack-to-rack interconnects in data center applications, 40-100 Gbps Ethernet and numerous specialty applications where radio frequency interference (RFI) and other environmental issues favor optical interconnection. A current rule-of-thumb for data centers is to use copper wires for lengths shorter than 3 meters and optical fibers for anything longer than 3 meters. For high-performance computation (HPC) systems, the rule is photonic interconnection for all lengths > 0.05 meters. This electrical-to-optical (E-O) technology transition will move inward as data rates exceed 100Gbps/channel, or where the compelling advantages of photonics: lightweight, less power consumption, lower cost per bit, are determining. On-chip Al and Cu wires are constrained on the short side by power density and on the long side by latency and loss. The only viable solution is increasing use of photonic circuitry near the central processing unit (CPU) or application-specific integrated circuit (ASIC) and outward, ideally with seamless on-chip/off-chip photonics, rather than converting signals from electrons to photons *outside* the package. Photonic interconnection is currently being accomplished with a range of multichip solutions, including Si, GaAs and InP devices in various transceiver modules and active cable assemblies.

Aggregate interconnection data rates of Tbps and Pbps will be required (1,000 – 10,000 Gbps) within this decade. This transition to photonics will still require parallel system buses, aiming toward 100Gbps/channel. These interconnects will be needed in larger, increasingly complex data center, router, switch, computer server-storage equipment and scientific computer applications. Integrated photonic technology will be required to scale system performance without enduring massively parallel Cu circuits and their attendant high power budgets and increasing system costs. Great strides have been made in adopting Si electronic device technology to photonic lasers and detectors. Commercial introduction of these developments has been limited to a handful of major Si IC manufacturers. A number of datacom system players, E-O transceiver, and value-added

connector manufacturers are providing what might be classified as interim solutions in this area. Universal industry goals are i) to achieve acceptably low power budgets; ii) to provide photonic signaling in the Tbps range, and iii) to use lower cost Si/CMOS capabilities, including existing processes where possible, to reduce the cost of photonic systems to the silicon IC paradigm.

The Integrated Photonic Systems Roadmap is a dynamic process, evident by the evolution of industry-wide semiconductor roadmaps over many years. The International Technology Roadmap for Semiconductors (ITRS) has reflected the semiconductor industry's migration path from *geometrical scaling* to *equivalent scaling*. *Geometrical scaling* (e.g., Moore's Law) has guided targets for the previous 35 years, and will continue in many aspects of chip manufacture. *Equivalent scaling* targets improving performance through innovative system-level design, process, and software solutions that will increasingly guide the semiconductor industry in the future. Function-driven design requires the incorporation of intelligent elements in the form of microprocessors, memory, and programmable logic devices built in silicon-based CMOS technologies. The *downscaling* of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. However, many quantitative requirements, such as power consumption and communication bandwidth no longer scale with Moore's Law.

Integrated Silicon Photonics research, development and commercialization initiatives address new functionalities that do not necessarily scale according to "Moore's Law".

- SiPh packages containing Si detectors, GaAs and InP lasers in SiP or PoP multi-chip designs.
- Fully integrated ICs that may in the future contain CPU/ASIC and Si photonic transceivers.

The so-called More-than-Moore approach typically allows for these functionalities to migrate from board-level modular applications, such as discrete transceiver packages and board-level interconnects, into a package-level (SiP), chip-level (SoC), Stacked Chip SoC (SCS) or Package-on-Package (PoP) solutions. What will a fully integrated Si-Photonic subsystem look like; and what are its design objectives? Table 1 depicts a likely path for this technology transition: discrete devices, to hybrid package assemblies, to integrated die functionality, to integrated photonic system-on-chip. Table 2 shows the projected integrated silicon photonics component deployment timeline.

Table 1. Silicon Photonics Technology Deployment

2015-16	2017-20	2020-25	Beyond
Discrete Devices	Interposers	EO CPU/ASIC	Logic-Memory-IO Integrated SiPh SoC Photonic Systems
EO Transceivers	InP VCSEL	Si Lasers	
Interconnect Modules	EO SiP/PoP	Multi-Die SiP	
MM Connectors	Fly-Over Cables	EO/Waveguide PCB	Wafer-Panel Substrates
MM Cables	MM-SM Connectors	SM Connectors	IO Connectors
AOCs	MM-SM AOC	SM Cables	Future WG

Interconnects Packaging SiPh Integration

Table 2. Silicon Photonics Components and Applications

Technology	Status
2015-16	
GaAs Lasers	VCSEL arrays commercially deployed in datacom
InP Lasers	Edge emitter arrays commercially deployed in telecom
Ge-on-Si Lasers	Research demonstration by several labs
Ge-on-Si Detectors	Fully waveguide integrated, commercially deployed
Waveguides	Si, SiON, SiN commercially deployed
SiP/SoC Assembly Technology	Electronics, but not photonics
Si Photonic Integration	Commercially deployed in cable and board assemblies
2017-20 Projected	
Ge-on-Si Lasers	Early market entry
Ge-on-Si Detectors	Pervasive commercial deployment
Waveguides	Pervasive commercial deployment, single channel
SiP/SoC Assembly Technology	Early 2.5 D deployment
Si Photonic Integration	Pervasive commercial deployment: cables and boards
2020-25	
Waveguides	Pervasive commercial deployment: WDM
SiP/SoC Assembly Technology	Pervasive commercial deployment: cables and boards
Si Photonic Integration	Emerging chip-to-chip intra-package
Beyond	
SoC Assembly Technology	Embedded in distributed circuit/system architectures
Si Photonic Integration	Transceiver-less: embedded electronic-photonic synergy

PACKAGING OF ELECTRONIC PHOTONIC SYSTEMS

The global network requirements are changing with the rise of the IoT and the migration to the cloud of data, logic and applications. These changing requirements must be accommodated while maintaining the pace of progress in size, cost and power per function that we have enjoyed for the last 50 years based primarily on the benefits of Moore's Law scaling of CMOS electronics. The introduction of photonics into the transmission, processing and even the generation of data through optically based technologies is a key enabling factor for continued progress as the benefits derived from Moore's Law scaling begin to slow.

Packaging is a limiting factor in electronics today since it has not kept pace with Moore's Law in scaling. Today electronic packaging is more expensive than the package contents in many cases and it contributes substantially to increased power requirements and latency. The solution to these limiting factors is a work in process with innovations such as wafer-level packaging (WLP), SiP architecture, 3D integration and heterogeneous integration. The integration of photonics into these emerging electronic packaging solutions is a focus of this Chapter but continued innovation in other areas will be essential.

There will be many specific challenges in realizing the benefits of integrating photonics into the fabric of the global network and the components attached to it. The solutions, however, cannot come from just packaging photonic components. The co-packaging of electronics, photonics and plasmonics will be required to address these substantial new challenges to meet the expanding requirement for higher performance, higher reliability, increased security, lower latency and lower cost in the future. The packaging of PICs will face the same challenges faced in packaging electronic ICs with the added complexity of integrating both active and passive photonic elements. Wherever possible industry must adopt and adapt the packaging technologies developed for electronics to decrease cost and time-to-market for the packaging of individual PIC circuits and incorporating PIC circuits and other photonic components into the complex 3D SiP through heterogeneous integration.

There will be new device types, new materials, new package production processes and new equipment required to accomplish these objectives. Some of these required innovations we know today but many specifics that must be addressed over the next 15 years are yet not known. The objective of this Roadmap Chapter is to identify packaging challenges with sufficient lead time so they solutions can be identified and proven before they become roadblocks to the pace of progress for the industry.

CONNECTORS

Silicon photonics technology (SiPh) is defined as photonic (lightwave) circuitry that employs low-cost Si as a device and circuit platform and that employs heterogeneous micro-packaging of various photonic chips and devices including GaAs, InP, and preferably Si micro-laser technology to drive low-cost/high-volume Computer/Datacom/Networking/Video Streaming applications. The compelling requirement for these technologies will be increasing circuit speed and bandwidth. These requirements are surfacing in high-performance computing, data communication networks, and data centers. Terabit speeds will be necessary by the 2020s. OEMs recognize this paradigm shift from Cu to photonic circuitry. OEMs such as Cisco Systems, IBM and Intel are working on these technologies at the chip and system level. Intel has announced its Omni Path Interconnect Architecture that will provide a migration path between Cu and Fiber $\geq$ 40Gbps.

The Interconnect TWG encompasses the following Technologies:

- Existing and Fiber Optic Connectors where the focus is on single-mode fiber (SMF),
- Future EO Sockets and/or Interposers (E-O conversion from metallic IC packages),
- Existing and Future fiber-optic Cables and Transceivers [Active Optical Cables (AOCs), board-level transceivers], and ???

Crosscutting Technologies covered in the Packaging TWG include:

- Interconnects within a SiPh SiP Package (Packaging TWG),
- Substrates employed in SiPh Multi-Chip IC Packaging (Packaging TWG),
- Direct Chip Attachment of SM FO Cables (SiPh Device TWG), and
- Technologies Employed within the Semiconductor and IC Packaging Industries (Above).

Probable Future Technology Needs in the Interconnect TWG include:

- Surface Mount Silicon Photonics for High-Speed and -Bandwidth (≥THz) Data Center/ HPCC applications, and
- Silicon Photonics MM fiber in Internet2, IoT, Industrial, Medical, and Department of Defense (DOD) applicationsfor noise-immunity, environmentally rugged high-speed and bandwidth applications.

Probable Future Interconnect Product Designs (*and Challenges*) include:

- SMF, PCB, IO Connectors (*Field Termination; Cost Targets*),
- InP/Si RX/TX: Board-Level Modules, Active Cables (*MM Designs in Production; SM Future*),
- Board Level Embedded Waveguide Connectors (*None Existing; Technology/Assembly/Cost*),
- EOPCB with embedded waveguide and interconnect technologies, and
- Chip to substrate or interposer electrical IO bump (copper pillar) densities down to <10 micron pitch from the ~50 micron in use today.

SUBSTRATE TWG

The two dominant types of substrates used in electronic systems are Organic Rigid Multilayer PCBs and Flexible PCBs. Both can be “active” or “passive” and all are custom engineered for each application, unlike connectors, which have many standard designs. The closest a PCB comes to high-volume are the motherboards designed by Intel and others for the desktop PC. The driving force in high-volume substrate manufacturing is to choose the technology, materials and design that will result in reliable products at the lowest cost.

The critical step in a reliable design is to select a material system which addresses the difference in the coefficient of thermal expansion (CTE) between silicon and glass to organic substrate and organic board. Historically there has not been an integrated system design between device, package, and printed circuit board. A system approach will be needed as we integrate more and

more system functions into the lowest level of packaging in order to achieve performance and cost goals. At some point in the next five years there will be a need to begin integrating a cost-effective method for single-mode optical interconnections at the board level. This implementation will require manufacturing process development, but more importantly the development of materials that meet the optical performance needs, produce minimal impact on the existing PCB manufacturing base, and meet the low-cost requirements.

ASSEMBLY TWG

The overall cost, including the cost for Assembly, of optical devices needs to be reduced substantially so that optical products are cost effective in more applications. An obvious way to avoid assembly cost is to minimize the number of parts to be assembled. That is being addressed through the increased use of integration. Unfortunately, all of the functions needed in optical applications cannot be integrated yet so assembly, or heterogeneous integration as it is often called, is needed.

Many of the most important potential applications require single-mode optical technologies where the assembly of parts requires tolerances and stability of the optical chains over the lifetime of the product in the operating environment with overall movements less than 1 micron. Achieving that level of mechanical consistency requires starting with the design, selecting materials and structures to minimize the effect of temperature and stress and other environmental phenomena, selecting materials, joining methods, and assembly processes that will yield that result. Generally, materials with high modulus and low TCE are best and have been used extensively in optical devices. Unfortunately these materials tend to be expensive so much effort is devoted to utilizing lower-cost materials and lower-cost processes.

Detailed mechanical and optical properties of the materials used in optical products are often not available. Standardizing on those materials and making the properties available will enable designers to model optical products more accurately thus minimizing the need to build and test many hardware configurations.

Assembly methods and equipment from the microelectronics industry are often the initial choices considered for manufacturing optical products. Many of these processes are perfectly suitable for optical devices, especially the electronic and non-dimensionally critical functions. In addition, a subset of the electronic methods are effective for the high-stability design and assembly methods. The chapter emphasizes the character of joining methods and highlights those standard processes, materials and equipment that are suitable for that demanding requirement. Thermocompression bonding, welding and UV cured polymers are often good choices.

Processes to achieve the 0.1 micron tolerances required for true passive alignment of optical devices are not widely available. Many approaches are being investigated to fulfill that need and avoid expensive (because it is “slow” and requires expensive equipment) active alignment where the optical chain is activated and used to actually ensure alignment is adequate.

Equipment to achieve the <0.1 micron of accuracy is not yet readily available. What is available is equipment able to achieve 0.5 micron accuracy. That capability needs to be improved. To capitalize on the resulting equipment, other steps are needed; overall design, inclusion of fiducials and reference points, selection of stable joining methods and joining materials, etc. In addition, improved interfaces to equipment are needed. These interfaces must reduce programming, setup and change-over times to minimize the cost to build a high mix of low-volume optical products.

TEST TWG

The IPSR Test TWG addresses overall lifetime test issues resulting from the inclusion of photonic capabilities into devices and products. Its emphasis is on silicon wafers and dies with photonic functionality and assemblies and products that include these devices. SiP assemblies and systems are addressed to the extent viable given the diversity of test needs that are specific to applications. The test issues for wafers, die, SiPs, and systems will be addressed at the Design, Qualification, Validation, Production, and In-Use stages of product life cycles[2]. Current and anticipated optical parameters to be tested and their value or level are considered along with the test access issue at each stage of the product life cycle.

Telecommunications test equipment, components, and methods have been and will continue to be adopted for the optical testing of products used outside of long-haul applications. Traditional methods are being extended and new methods developed to address test needs for photonic wafers, photonic integrated circuits, and SiP that utilize optics and complete systems. Utilizing these extended methods requires optical probing of both wafers and dies combined with electrical probing resulting in a series of mechanical issues. The inclusion of optical probing, especially single-mode probing, requires gratings or other access points on wafers. For individual die, dual-mode (electrical and optical) probing is especially difficult due to the small size of die and difficulty of holding and locating probes accurately. At the SiP level, the problems are easier because the device is larger, not as fragile, and is often designed to facilitate dual-media probing. The wafer, die, and SiP probe fixtures tend to be expensive due to the complexity and accuracy required. System level test access is usually easier because at that level, electrical interfaces and optical connectors are included as part of the device under test (DUT).

In addition to probe access, optical test methods to simultaneously characterize and compare multiple optical lanes and or ports at the same time are needed. One need is comparative simultaneous testing of multiple signals from arrays of ribbon fibers, waveguides or chip sources or detectors for optical skew, jitter, etc. A related need is simultaneously evaluating optical signals multiplexed on one fiber or waveguide. Applications with arrays of up to 256 ports (fibers, waveguides chips) or ~256 multiplexed wavelengths are forecast in the next ten years.

In addition to the standard telecom optical parameters [power, wavelength, attenuation, jitter, signal-to-noise ratio (SNR), etc.], emerging applications utilize virtually every parameter that light can have, potentially requiring the extension of test capability in multiple dimensions such as polarization, phase noise, spatial modes, multiple fiber cores, etc. While these emerging needs are potentially very broad, the near-term emerging needs seem most likely to be extensions of data communications needs.

Optical communication applications are likely to utilize wavelengths ranging from 650 to 1700 nm, multiplexed together with channel-to-channel spacings as close as 25 GHz, detector efficiencies of ~1Amp/Watt, receiver sensitivities as great as -45 dBm, and power levels of 1 watt or less. With wider channel spacings symbol rates of 100 Gbaud per lane, modulation schemes

[2] Testing and evaluation during PIC fabrication is specifically excluded and left for the Monolithic Photonic Integration chapter.

utilizing up to 10 bits per symbol, polarization multiplexing, bit-error rates (BER)s of 10^{-12}, etc. are possible. Over time these parameters will improve so test capabilities will need to stay ahead of them. Data rates as high as 500 Tbps per fiber are likely to emerge in the next ten to 15 years.

Design for test by including optical test access points, Built-In Self Test (BIST), redundancy for self repair, and prognostics to report changes and deterioration during operation over the life cycle of optical products are desirable and of value in an increasing number of applications. These tests should be considered for inclusion not only in designs, but also in software design tools as well.

PHOTONIC SENSORS TWG

The Photonic Sensors TWG focuses on photonic chip-scale and systems-level devices for the detection of chemical and biological targets, and on physical and environmental sensing systems. The TWG evaluates the intersection of materials, cost, and performance requirements, as well as integration with sample processing and analysis. While the primary goal of the TWG is to map manufacturing development for the near-term (5-year) time frame, the group also considers developments needed over a 20-year period. The co-chairs of this IPSR TWG are Ben Miller: benjamin_miller@urmc.rochester.edu and Anu Agarwal: anu@mit.edu

The TWG is currently developing the roadmap. The complete roadmap will be provided at a later date.

ELECTRONIC PHOTONIC DESIGN AUTOMATION (EPDA) TWG

The EPDA TWG focuses on improving the design methodologies for scalable integrated electronic-photonic design. One of the overarching goals for improved methodologies and design tools [e.g., electronic design automation (EDA) and photonic design automation (PDA) software] is to enable the many electronics IC design teams of the world to integrate photonic functions into their systems/ASICs/SoCs without requiring low-level physics design and photonics PhDs on their staff. Thus the overall goal is to make integrated photonics design easier by putting the low-level physics burden into the design tools and models. Another goal is enabling a robust photonics IP market. This includes analyzing existing methodologies and defining better ways (or standards) for the various forms of design data to move between the various design "steps" of a methodology. The chair of this IPSR TWG is Brett Attaway: battaway@sunypoly.edu

The TWG is currently developing the roadmap. The complete roadmap will be provided at a later date.

WORKFORCE DEVELOPMENT AND EDUCATION TWG

AIM Academy has formed a Technology Working Group to identify the Education and Workforce Development needs to support the development of a world-class integrated photonic systems manufacturing industry in the United States. The first step in creating the roadmap has been to identify cross-cutting Workforce Development and Education needs in a table along with the other IPSR TWGs. The next step will be to identify needed learning activities.

Table 3. Cross-cutting needs with other IPSR TWGs

Project Categories/Target Audiences	2017	2018	2020	2025	2030
Outreach/K-12	Career Information				
Certificate, Competency-based Program/Associate of Science, Associate of Technology		Test			
		Assembly			
			Substrates		
			Connectors		
Industry Internships/BS		Monolithic Integration			
Industry Internships/MS	Monolithic Integration				
		Test			
		Assembly			
		Electronic-Photonic Design Automation (EPDA)			
		Packaging of Electronic-Photonic Systems			
		Photonic Sensors			
			Connectors		
			Substrates		
Certificate, Apprenticeship, Degree program/PhD	Monolithic Integration				
	Electronic-Photonic Design Automation (EPDA)				
	Packaging of Electronic-Photonic Systems				
	Photonic Sensors				
		Test			
		Assembly			
		Connectors			
		Substrates			
Certificate, Workshop, On-site Retraining/Current employees	Assembly				
	Test				
	Monolithic Integration				
	Electronic-Photonic Design Automation (EPDA)				
		Packaging of Electronic-Photonic Systems			

The chair of this IPSR TWG is Brian Anthony: banthony@mit.edu

The TWG is currently developing the roadmap. The complete roadmap will be provided at a later date.

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We extend special acknowledgment to those contributors who drafted, edited, and summarized the materials in this document:

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- Nicolaus Rhenwrick, Lockheed Martin
- Katharine Schmidtke, Strategic Sourcing Manager, Facebook
- Irene Sterian, Executive Director, ReMAP, Celestica
- Lionel Kimerling, MIT, Ex-Officio Member
- Robert Pfahl, IPSR, Ex-Officio Member

Technology Working Groups and Product Emulator Group Members.

The Technology Working Groups (TWGs) and Product Emulator Groups (PEGs) include a large number of industry, academic and government professionals. Members of each TWG are listed at the end of each Technology Roadmap. A complete list of roadmap participants can be found in Appendix B. Seven hundred professionals from more than 16 countries and representing 254 organizations took the time to participate actively in the IPSR/PSMC Roadmapping process through the TWGs and PEGs or during four roadmapping workshops and webinars. Although we value the work of all participants and have made every effort to include them in these acknowledgments, probability dictates that a few organizations and/or individuals may have been left out. If that is the case, we apologize for any inadvertent oversight. Please note that the professional participants listed are respected as visionaries in their respective fields, and their views are not necessarily a reflection of the views of the entities where they work. The following list identifies the IPSR leaders who are chairing the TWGs and PEGs:

IPSR Leadership Committee

- Robert C. Pfahl, Jr., Director of Roadmapping AIM Academy, iNEMI

  Chair, IPSR Data Center Product Emulator Group (PEG)

  Chair, IPSR Automotive PEG

- Lionel C. Kimerling, MIT, Education, Workforce Development and Roadmap Executive, AIM Photonics Institute

  Chair, IPSR Monolithic Integration Technology Working Group (TWG)

- Bill Bottoms, Third Millennium Test Solutions,

  Chair, IPSR Integrated Photonics Packaging TWG

- Richard Otte, Promex Industries,

  Chair, IPSR Assembly (and test) TWG

- John L. MacWilliams, US Competitors

  Chair, IPSR Connectors (and Substrates) TWG

- Richard Grzybowski, MACOM,

  Chair, IPSR Internet of Things (IoT) Product Emulator Group (PEG)

- Chris Coleman, Keysight Technologies

  Co-Chair, Test TWG

- Voya Markovich, Advanced Hardware Consulting

  Chair, IPSR Substrates TWG

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  Co-Chair, Emulator Cost Modelling

- Ben Miller, University of Rochester,

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- Brett Attaway, AIM Photonics Institute

  Chair, IPSR Electronic Photonic Design Automation TWG

- Arthur Paolella, Photonics Program Manager, Harris Corporation

  Chair, RF Photonics PEG

- Brian Anthony, AIM Photonics Academy

  Chair, Workforce Development and Education TWG

Firms Contributing to the 2016 Integrated Photonic Systems Roadmap

Organizations from throughout the global supply-chain participated in developing this roadmap. The following list gives a breakdown of their role in the supply chain.

END USERS
Facebook
Microsoft
Verizon

ORIGINAL EQUIPMENT MANUFACTURERS (OEM)
AEPONYX
Broadcom
Ciena
Cisco Systems IncGE Global Research
Harmonic
Hewlett Packard Enterprise
Huawei Technologies
IBM Corporation
Imaging Solutions Group
Intel Corp.
Juniper Networks
LGS Innovations
Nippon Telegraph and Telephone Corp.
Nokia-Bell Labs
Oracle
Philips
Plexxi, Inc.
Toshiba

DEFENSE CONTRACTORS
Boeing
Harris
Lockheed Martin
Raytheon
Rockwell Collins
United Technologies Corp

ELECTRONIC/PHOTONIC MANUFACTURING SERVICES (EMS)
Celestica, Inc.
Chiral Photonics
Morton Photonics
MTEQ, Inc.
Photon Gear
Plexus
Promex Industries
Sanmina Corp.
SunSil Inc

TEST EQUIPMENT MANUFACTURERS
3MTS, Inc.
Advantest Corp.
Keysight Technologies
Luna Inc.
Tektronix

ASSEMBLY EQUIPMENT MANUFACTURERS
Amrica
ficonTEC (USA) Corporation
Finetech
Kulicke & Soffa
MRSI Systems
New Scale Technologies, Inc.
Palomar Technologies
Tokyo Electron
Universal Instrument

SEMICONDUCTOR EQUIPMENT MANUFACTURERS
SAMCO
Ebara Technologies Inc.
EV Group
Semsysco

TRANSEIVER SYSTEM/COMPONENT SUPPLIERS
Acacia Communications Inc.
Archcom Technology
Avago
Enablence Technologies Inc.
Finisar Corp.
Hisense Broadband Multimedia Technologies Co
HOYA Xponent
Luxtera Inc
NEL America
Oclaro Inc.

ROUTER AND SWITCH SUPPLIERS
CoAdna Photonics, Inc.
Compass EOS
Mellanox Technologies

LASER & LED SUPPLIERS
LaserMax
TeraDiode, Inc
TeraXion

ELECTRONIC PACKAGING SUPPLIERS
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Quik-Pak
Tessera

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JENOPTIK

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TTM

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Fujikura Ltd.
Harting
Molex
Nufern
OFS
Samtec Ltd
Senko Advanced Components.
Sumitomo Electric Industries, Ltd.
TE Connectivity
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Physik Instrumente
Lumetrics
Optimax Systems

MATERIAL SUPPLIERS
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Asahi Glass
Corning Inc.
Dow Corning
Dow Electronic Materials
Henkel Corporation

MATERIAL SUPPLIERS, Cont'd
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Metalor
Namics Corporation
SABIC
Shinko
SunEdison Semiconductor
TOK

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FABLESS SEMICONDUCTOR/PHOTONIC MANUFACTURERS
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SiFotonics Technologies
Sonas Systems Inc.
Xilinx

HETEROGENEOUS INTEGRATION OF InP MANUFACTURER
Aurrion

DESIGN TOOLS
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Cadence
CMC Microsystems
Lumerical Solutions, Inc.
Mentor Graphics
MERL (Mitsubishi Electric Research Labs)
Optic2Connect
PhoeniX Software
Synopsys, Inc.

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AIST
Ceramics Corridor Innovation Center
COBO
CPMT
iNEMI
Institute for Defense Analyses
Heterogeneous Integration Roadmap
Integrated Photonic Systems Roadmap
ITRS
MIT Microphotonics Center
PETRA
ReMAP
SEMATECH

UNIVERSITIES/RESEARCH INSTITUTES
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Ayar Labs
Baker College
Berkeley Wireless Research Center
Boston University
Columbia University
Dartmouth College
Draper Laboratory
Fraunhofer HHI
Fraunhofer IZM
George Washington University
Georgia Institute of Technology
Ghent University
Graduate School for the Creation of New Photonics Industries
Hong Kong University of Sci & Tech
IMEC
ITRI
LETI
MATEC
McMaster University
MIT

UNIVERSITIES/RESEARCH INSTITUTES, Cont'd
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MIT Deshpande Center
MIT EMAT
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NICT/Waseda University
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Rutgers University
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Stanford University
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SUNY-CNSE
Texas A&M University
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TU Eindhoven
Tufts
Tyndall National Institute
U. Delaware / MIT
UC Berkeley
UC Davis
UC Los Angeles
UC San Diego
UC San Francisco
UC Santa Barbara
UMass Boston
UMass Lowell
Università di Modena e Reggio Emi
Università di Pavia
University of Arizona
University of British Columbia
University of Pittsburgh
University of Rochester
University of Southern California
University of Southampton
University of Tokyo
University of Toronto

COMMUNITY COLLEGES
OP-TEC
Quinsigamond Community College

FEDERAL AGENCIES
Advanced Manufacturing Policy Office
Air Force Office of Scientific Research
Air Force Research Laboratory
MIT Lincoln Laboratory
NASA Goddard Space Flight Center
National Institute of Science and Technology
National Research Council of Canada
National Science Foundation
NIST
OSD ManTech
Sandia National Laboratories
U.S. Army Research Laboratory
U.S. Army Night Vision Laboratory
U.S. Navy NAVAR
U.S. Naval Research Laboratory

TRADE ASSOCIATIONS
ECIA
IPC
OSA/OIDA
Semi
Semiconductor Industry Association (SIA)

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