Integrated Photonics
Grand Challenges and Key Needs for 2018

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MIT
AIM Photonics Institute
IPSRI-International Webinar: December 21, 2017

Data Centers – 3D/Augmented Reality/Automotive – 5G/IoT

integration – standardization – cross-market platforms
- Integrated Photonics Technology supply chain
Challenges and Needs for 2018

- Critical Themes (3-10)
  - *Functional Blocks* - Platforms – System Level Design

- Economics (10-16)
  - *Demand* – Component-to-System Cost - Reliability

- Technology (17-30)
  - TxRx (DC) - RF Signal Processing (5G) - *e-p Synergy*
  - *Sense: sampling and signal interpretation*

- Manufacturing (31-34)
  - *Standardization* – Consolidation - *Coordination*

- Success in 2018 (35-36)
  - *Continuity*: electronics-photonics-integration

Outline: Economics, Technology, Manufacturing
Infrared laser projector components: i) a vertical-cavity surface-emitting laser or edge-emitting laser, ii) wafer-level optics, and iii) diffractive optical elements.

Technologies: multipoint CMOS imaging; ToF mapping; structured light; phased arrays.

Outline: Economics, Technology, Manufacturing
Silicon Photonics is the “future proof”, modular solution for SM-WDM bandwidth density scaling.

- **increases**: yield, reliability, density
- **reduces**: cost, *time to market*, power, latency

*Integrated Photonic Systems Roadmap 2016*
Integrated Photonics: 2018 Priorities

- **Automated Design**
  - validated PDK models: e-p circuits and systems
  - foundry infrastructure: IP licensing/indemnification

- **Monolithic Integration**
  - heterogeneous SM functional blocks

- **Optical Packaging**
  - on-chip/off-chip; interposer; on-board parallelism
  - parts supply chain; known failure modes

- **Test**
  - Design-for-Test; BIST; high throughput

Outline: Economics, Technology, Manufacturing
The Road to Silicon e-p Synergy

**Outline:** Economics, Technology, Manufacturing

<table>
<thead>
<tr>
<th>Technology</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2015-16</strong></td>
<td></td>
</tr>
<tr>
<td>GaAs Lasers</td>
<td>VCSEL arrays commercially deployed in datacom</td>
</tr>
<tr>
<td>InP Lasers</td>
<td>Edge emitter arrays commercially deployed in telecom</td>
</tr>
<tr>
<td>Ge-on-Si Lasers</td>
<td>Research demonstration by several labs</td>
</tr>
<tr>
<td>Ge-on-Si Detectors</td>
<td>Fully waveguide integrated, commercially deployed</td>
</tr>
<tr>
<td>Waveguides</td>
<td>Si, SiON, SiN commercially deployed</td>
</tr>
<tr>
<td>SiP/SoC Assembly Technology</td>
<td>Electronics, but not photonics</td>
</tr>
<tr>
<td>Si Photonic Integration</td>
<td>Commercially deployed in cable and board assemblies</td>
</tr>
<tr>
<td><strong>2017-20 Projected</strong></td>
<td></td>
</tr>
<tr>
<td>Ge-on-Si Lasers</td>
<td>Early market entry</td>
</tr>
<tr>
<td>Ge-on-Si Detectors</td>
<td>Pervasive commercial deployment</td>
</tr>
<tr>
<td>Waveguides</td>
<td>Pervasive commercial deployment, single channel</td>
</tr>
<tr>
<td>SiP/SoC Assembly Technology</td>
<td>Early 2.5 D deployment</td>
</tr>
<tr>
<td>Si Photonic Integration</td>
<td>Pervasive commercial deployment: cables and boards</td>
</tr>
<tr>
<td><strong>2020-25</strong></td>
<td></td>
</tr>
<tr>
<td>Waveguides</td>
<td>Pervasive commercial deployment: WDM</td>
</tr>
<tr>
<td>SiP/SoC Assembly Technology</td>
<td>Pervasive commercial deployment: cables and boards</td>
</tr>
<tr>
<td>Si Photonic Integration</td>
<td>Emerging chip-to-chip intra-package</td>
</tr>
<tr>
<td>SoC Assembly Technology</td>
<td>Embedded in distributed circuit/system architectures</td>
</tr>
<tr>
<td>Si Photonic Integration</td>
<td>Transceiver-less: embedded electronic-photonics synergy</td>
</tr>
</tbody>
</table>

**700 contributors**

**254 organizations**

**16 countries**

*InP, SiN (GaN) are important to an emerging heterogeneous e-p platform.*
Supply Chain Coordination

Outline:
- Economics,
- Technology,
- Manufacturing

- Extend this table to **3D waveguide (industry expects this to happen by 2020)**
- Extend this table to independently **routable optical layers** (vertically integrated WG)
- **Integration level complexity** to be added
- Study **cost scaling at system level**

Ajey Jacob, Global Foundries
co-chair, Monolithic Integration TWG

Outline: Economics, Technology, Manufacturing
Supply Chain Coordination

Table 5. Photodetector integration roadmap

<table>
<thead>
<tr>
<th>Key Attribute</th>
<th>Parameter</th>
<th>Description</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2025</th>
<th>2035</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absorption</td>
<td>α (cm⁻¹)</td>
<td>loss @ 1550nm</td>
<td>10⁴</td>
<td>10⁴</td>
<td>10⁴</td>
<td>10⁴</td>
<td>10⁴</td>
</tr>
<tr>
<td>Dark Current</td>
<td>I (nA)</td>
<td>interface + bulk</td>
<td>0.2</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>Process Integration</td>
<td>cm⁻²</td>
<td>dislocation density</td>
<td>10⁷</td>
<td>10⁷</td>
<td>10⁶</td>
<td>&lt;10⁵</td>
<td>0</td>
</tr>
<tr>
<td>Efficiency (p-i-n)</td>
<td>R (A/W)</td>
<td>responsivity</td>
<td>1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>Bandwidth (p-i-n)</td>
<td>B (GHz)</td>
<td>B @ 1550nm</td>
<td>40</td>
<td>67</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Gain x Bandwidth (APD)</td>
<td>GB (GHz)</td>
<td>GB @ 1550nm</td>
<td>300</td>
<td>400</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Guided Power</td>
<td>mW</td>
<td>~linear response</td>
<td>30mW</td>
<td>100mW</td>
<td>100mW</td>
<td>100mW</td>
<td>100mW</td>
</tr>
</tbody>
</table>

Table 6. Modulator integration roadmap

<table>
<thead>
<tr>
<th>Key Attribute</th>
<th>Parameter</th>
<th>Description</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2025</th>
<th>2035</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate</td>
<td>Gb/s</td>
<td>OOK rate</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Extinction Ratio/Insertion Loss</td>
<td>dB/Δα</td>
<td>Δα/α</td>
<td>2</td>
<td>2.5</td>
<td>3</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Spectral Range</td>
<td>nm</td>
<td>@ Δα/α spec</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Spectral Efficiency</td>
<td>b/Hz</td>
<td>DP-QAM</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

To be added in 2018: specification of Materials and Tool performance

Ajey Jacob, Global Foundries co-chair, Monolithic Integration TWG

Outline: Economics, Technology, Manufacturing
Long discussion on reliability. Agreed to keep the current numbers.

Ajey Jacob, Global Foundries co-chair, Monolithic Integration TWG

Outline: Economics, Technology, Manufacturing ... Questions?
Will the Data Center market support the required R&D and drive adoption of integrated photonic technology?

Key needs

- platforms that leverage R&D investments
- standards that limit R&D risk
- manufacturing infrastructure for high volume ramp
Case Study: Transceiver

Hardware
- Server Racks, Switches, Optical Transceivers, Fibers, Building Facilities (Shell, Power Supply, Cooling)

Software
- Platform-level Software, Cluster-level Software, Application-level Software

Set-up and Operation
- Development, Purchase, Installation, Electricity, Maintenance


The transceiver is part of the Data Center system.

W. Yu and R. Kirchain, MIT
$ sales to support R&D cost of one new product

R&D cost

0.15

Revenue To Support One Product R&D

For an estimated Silicon Photonics TAM of $200M, the industry product cycle is 1yr for one product!

For estimated Silicon Photonics revenues of $30M for one company, the product cycle is 3.3yrs!

W. Yu and R. Kirchain, MIT
Can sales from the Data Center sector support all new *industry* TxRx products?

<table>
<thead>
<tr>
<th></th>
<th># of Datacenters</th>
<th>Bisection Bandwidth Pb/s</th>
<th># of layers of transceivers</th>
<th>$/Gbps per transceiver</th>
<th>$M transceiver sales</th>
<th># of Products such sales can support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Google</td>
<td>15</td>
<td>5.2</td>
<td>4</td>
<td>1</td>
<td>312</td>
<td>1.5</td>
</tr>
<tr>
<td>Amazon</td>
<td>44</td>
<td>5.2</td>
<td>4</td>
<td>1</td>
<td>915.2</td>
<td>4.5</td>
</tr>
<tr>
<td>Microsoft</td>
<td>36</td>
<td>5.2</td>
<td>4</td>
<td>1</td>
<td>748.8</td>
<td>2.8</td>
</tr>
<tr>
<td>Facebook</td>
<td>~10</td>
<td>5.2</td>
<td>4</td>
<td>1</td>
<td>208</td>
<td>1.0</td>
</tr>
</tbody>
</table>

200G x 2 channels x 8 channels x OSFP x Si InP = 36 products >>

Mega-DCs can support 10 products each year.

1. High R&D cost + Market Fragmentation will support 36 product cycles of 3.6 yrs.

Economics

W. Yu and R. Kirchian, MIT
Shortage of components

“Shortages of high-end optics, such as EML and DFB laser chips, is the main limiting factor for 100GbE market growth in 2016.” – LightCounting.com

Limited production capacity

- High risk to make a multi-million investment before the accepted solution is announced.
- It takes time to add equipment and people into production line.

“People assumed they had time to ramp...[but] the industry has never seen such a ramp with optics.” – Andreas Bechtolsheim

2. Production ramp time to high volume production limits revenue.

Economics

W. Yu and R. Kirchain, MIT
R&D costs and production ramp rate determine Data Center revenue portion for integrated photonics.

- Cost and $/Gb/s will decrease with each new product technology.
- Ramp time to high volume production limits revenue.

W. Yu and R. Kirchain, MIT
The optical transceiver is a bottleneck due to cost and time.

- **Cost** is i) device cost with ii) full implementation cost of that technology solution.
- **Time** is i) time to sample plus ii) ramp time to high volume implementation.

Supply Chain coordination is critical to high volume production.

- Vendor and upstream supplier coordination
  - solution winner, *time scales* and volume.

The winning product should have an optimal combination of:

- performance, cost and *manufacturing scalability*. 

Economics ... *Questions?*
Building cross-market platforms

- **Transceivers**
  - *the transition to on-board optical interconnection*
  - MT connectors
  - optical interposers technology and cost

- **Analog RF optical signal processing**
  - transceivers: phase modulation
  - special purpose FFT processor: frequency channelization

- **Drivers for high level photonic integration**
  - coherent optical circuits
  - on-chip optical networks

- **Sensing and Optical Phased Arrays (>2018 AIM targets)**
Sequence of line card implementations for increased bandwidth

Nicholas Ilyadis, Broadcom
Before the benefits of silicon photonics can be realized, new high performance and cost effective solutions to optical packaging and connectorization must be developed.

- Optimum performance and functionality from silicon photonic devices and circuits require single mode (SM).
- SM requires precision alignment inside the package and in optical connectors.
  - expanded-beam (10um expanded to 80um) optical connectors relieve alignment and dust limitations
  - early entry for MM at short reach?

*Optical interfaces degrade performance and increase cost.*

Tom Marrapode, Molex
On-Board Optical Interconnection AIG

OBO AIG (Application Interest Group): 12 companies, international
Phase 1 complete in 2017; Phase 2 in 2018

Technology: TxRx
System Requirements

- Single-mode operation at SiPh operating wavelengths [1300, 1550 nm]
- Low propagation loss at SiPh operating wavelengths [$<\sim 0.01 \text{ dB/cm}$]
- Low polarization dependent loss (PDL) [$< 0.1 \text{ dB}$]
- Low-loss coupling to standard SM fibers
- Transceiver-to-transceiver loss small [$<\sim 3 \text{ dB}$]
- Ease of termination (low cost) in connectors and sockets
- Ease of routing from mid-board modules to board-edge connectors.
- Low sensitivity of optical properties to temperature & humidity
- Reflow compatibility (if embedded in PCB) [260 C]

*On-Board optical interconnection is an unsolved system problem.*

*Terry Smith, 3M*
Challenge: Optical Interposer

The purpose of an interposer is i) to spread a connection to a wider pitch, ii) to reroute a connection to a different connection, iii) to enhanced reliability and assure successful assembly.

- Needs low-loss waveguides (but easier than PCB)
- Needs new, cost-effective low-loss optical-coupling bond between photonic components and interposer waveguides.
- Increases system parts count.
- Increases system process steps.
- May require special handling (due to fragility, temperature sensitivity, etc.)
- May require manual attachment to PCB.

Terry Smith, 3M
Interposer Assembly Dominates Package Cost.

W. Yu and R. Kirchain, MIT
Functional Blocks

- **Transceiver**
  - power, bandwidth density
  - modulation format, polarization, spectral efficiency

- **RF Optical Signal Processor**
  - power, bandwidth density
  - notch filter, FFT

- **WDM Front End**
  - power, bandwidth density
  - temperature stabilization, e-p lambda lock
Interposer for FPGA Transceiver

- 25-Gbps error-free data link on a silicon optical interposer with an FPGA
- Transmitter pre-emphasis and receiver equalization
- Compatible with optical interconnect standards: OIF CEI-25G, 100GbE, 400GbE
- **Optical-pin/MM near term implementation**

Schematic diagram of an InP-based 500Gb/s PM-QPSK transmitter PIC and the active block PIC on the right.

- 10 tunable distributed feedback lasers
- 40 Mach-Zehnder modulators
- all required sense and control electronics.

Fred Kish, Infinera)
Integrated RF photonic filter

- low-loss silicon nitride circuit: ring resonators for pre-processing and optical filtering units
- low biasing of Mach-Zehnder modulator for link optimization to achieve low NF

- 8 dB RF gain
- noise figure: 15.6 dB
- spurious-free dynamic range: 116 dB
- rejection >50 dB in the stopbands


Technology: RF Signal Processor
Heterogeneous materials integration challenge: **monolithic, continuous process flow with associated economic advantages**

A. Paolella, Harris, IPSR 2016, RF Photonics Chapter
Functional Blocks

3mm x 6mm e-p chip

transmitter/receiver banks; coupler, photodetector, ring modulators
electronic–photonic system-on-chip: >70M transistors and 850 photonic components


Technology: WDM Front End
LSI Photonics: I/O for 32 bit Network

64 λ Node Multicore Core WDM Scenario at 1mm² per tile

Single Wavelength per Tile ID
- 64 λ WDM
- Si/SiO₂ HIC waveguide
- 40 wg – 32 data, 8 metadata
- Tile area used: 0.5mm²

Tile Transmitter
- 40 modulators for each core
- Single wavelength for all bit lines
- SiGe EA modulator & driver

Tile Receiver
- 63 ch. (N-1) receiver section per tile
- 40 one bit data lines
- 5um Ring Resonator Filters
- SiGe Detector integrated w/Filter

chip/package/board-level networks driving LSI silicon photonics

Technology: LSI Scaling ... Questions?
Building the Integrated Photonics Manufacturing Ecosystem
Si Wafer Processing Hub

- 1.3M ft² facility
- cutting edge 300/450mm toolset
- 135k ft² of class 1 capable cleanroom
- processing capability span 65nm - 7nm

- Years of proven silicon photonics results
- 300mm tools provide outstanding quality photonics
- 3D stacking w/CMOS
- Partnerships drive continuous revitalization investments

300mm Si Photonics Wafer

Manufacturing

Albany, NY
1. **Wafer-scale** photonics packaging
   - First-level interposer metallization
   - De-bond and dicing of wafers

   *70-80% of the cost of a Si-photonic system is in the package*

2. **Chip-scale** test, assembly and packaging
   - Laminate and fiber attach
   - High-speed test and BIST

*Rochester, NY*
<table>
<thead>
<tr>
<th>1 Year from now</th>
<th>3 Years from now</th>
<th>5 Years from now</th>
</tr>
</thead>
<tbody>
<tr>
<td>Funnel/vector students in related areas into IP start training from early on in school carrier market appeal of IP to draw interest short courses for broad Ed level (online/pre-recorded) short courses for specialized skills (higher education)</td>
<td>Offer lots of hands-on training to students (MS/PhD level first then BS) heavier marketing of IP appeal offer diversity in skills thoughts--specialty tracks on BS and MS offer IP focus programs: MS; BS--tracks students from early on degree</td>
<td>Have students ready to graduate who have been devoted to IP from the beginning</td>
</tr>
<tr>
<td>Establish working MPW model with working EDPA tools to enable R&amp;D ventures in Silicon Photonics</td>
<td>Establish product packaging solutions to target the various markets for optical products</td>
<td>Establish Packaging HVM capability to support volume growth to compete in worldwide markets.</td>
</tr>
<tr>
<td>Establish a baseline for full integrated photonics production. Provide initial training to access production runs.</td>
<td>Engage standard bodies for package processes. Successfully scale out PICs for larger volume production.</td>
<td>Broaden HVM applications beyond the datacom sector.</td>
</tr>
</tbody>
</table>

Manufacturing
Silicon Photonics: Fall AIM Tech Mtg

- **Chip fabrication**
  - Ge-epi at 45nm node: compatible thermal budget
  - optical I/O options: v-groove, optical pins
  - hermeticity
  - 300mm challenges: test, $C_{PK}$ and cost

- **Board-level Interconnection**
  - TxRx: pluggable (reliability) vs. surface mount (cost)
  - established solutions in system test
  - system requirement focus: interfaces (connectors)

- **Design at system level vs. chip shrink**
  - chip-package-module-system co-design

45nm is a compelling transition node for Silicon Photonics. Connectors limit on-board optical interconnection.
Key Technology Needs for 2018

- **Design**
  - robust Design-for-Yield; package simulation
  - functional blocks: RF-OSP, TxRx, WDM e-p front end
- **Monolithic Integration**
  - system requirements for switch and laser integration
- **Assembly**
  - alignment processes, tolerances and associated costs
- **Connectors**
  - Module-PCB and PCB-cable connectors
- **Packaging**
  - optical requirements for embedded package, vertical/edge access; board surface mount; hermeticity
- **Test**
  - Design-for-Test; in-line monitors

Manufacturing ... *Questions?*
Thank You
and Happy Holidays

Acknowledgements

- AIM Photonics Institute members
- IPSR International contributors
- MIT Microphotonics Center members
- iNEMI members
- OSA/OIDA members
- IEEE Photonics Society members
- SPIE Photonics West participants
- Photon Delta and the World Technology Mapping Forum TWGs