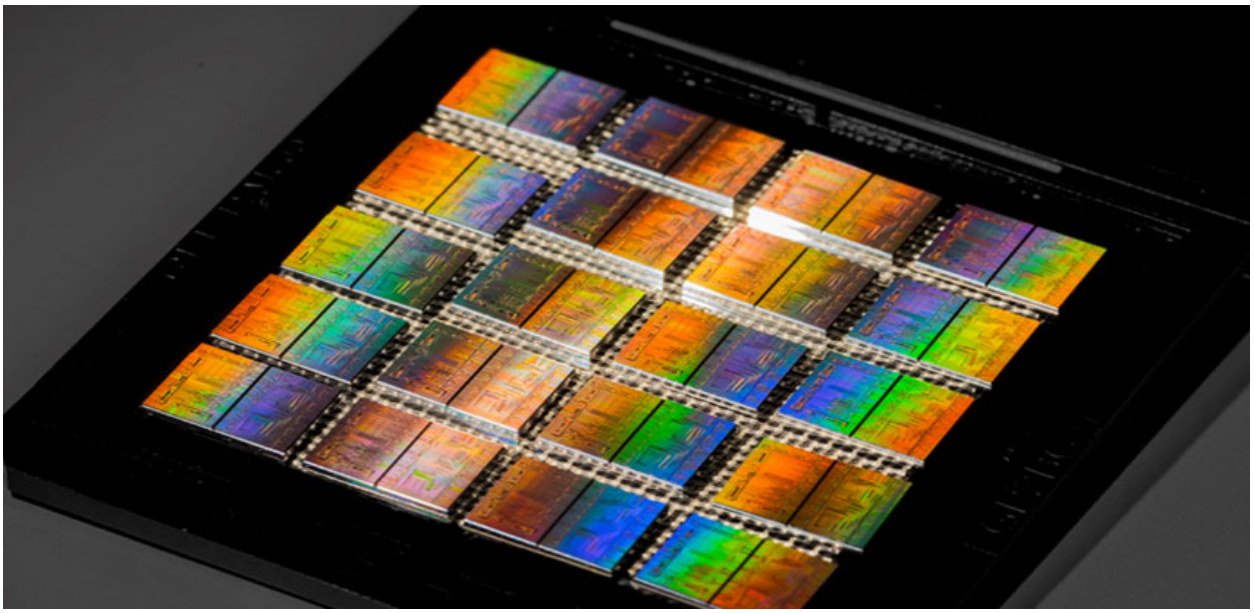
Knowledge and Innovation for Manufacturing Initiative - Integrated Photonics

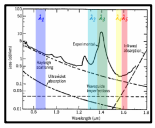


(Image courtesy M.L. Fanto. AIM Photonic chips designed by Precision Optical Transceivers and RIT Integrated Photonics Group)

Remote-education interactive online seminars on photonic integrated circuit principles, design, and systems applications.

APA1

Recommended pre-requisites: none



Photonics Fundamentals

An introductory overview on photonics materials trends for high-index contrast devices, and power- or data-rate design for a generic optical transceiver link. Materials topics include the origins and correlation of polarization and absorption, non-linear two-photon absorption, and band structure (band gap, carrier mobility) in semiconductors. Optical link topics include modal dispersion and group refractive index, Wavelength Division Multiplexing and channel spacing, power versus dispersion budget for a transceiver link. Design challenges address materials selection and routing architecture for an AS-PIC chip.

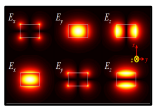
Instructor: Prof. L.C. Kimerling (MIT)

3 hrs

Starting proficiency: introductory background in optics, differential equations

APA2

Recommended pre-requisites: APA1



Passive Devices for Integrated Photonics

A primer on high-index contrast optical confinement in waveguides, and a survey of optically passive devices that exploit the photonics principles of mode-transformation, wave interference, and evanescent coupling. Waveguide topics include a brief review of the Helmholtz equation and its multimode or single mode solutions, polarization modes in two-dimensional optical confinement, and scattering loss versus refractive index difference. Devices briefly surveyed include inverse taper edge coupler, Y-splitter; grating coupler, Mach-Zehnder modulator; directional coupler, ring resonator. Design challenges address preliminary device design to configure passive components for an AS-PIC chip.

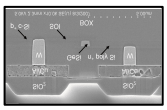
Instructor: Prof. J. Hu (MIT)

3.5 hrs

Starting proficiency: Maxwell's Equations, fiber optics technology or moderate photonics background in Group IV semiconductors

APA3

Recommended pre-requisites: APA1, APA2



Active Devices for Integrated Photonics

A survey of optically active device design to detect, modulate, and generate laser light for silicon-based integrated photonics circuits. Detector topics include responsivity and response time, p-i-n versus avalanche photodetector design, and waveguide coupling design. Modulator topics include electro-optic effect and electroabsorption devices, the latter focusing on Franz-Keldysh and Quantum Stark Confinement effects. Light generation topics include InAs quantum dot laser source on Si, Ge-on-Si lasers, GeSn infrared lasers, and the interposer approach to co-package III-V laser and Si PIC chips. Design challenges address preliminary device design to configure active components for an AS-PIC chip.

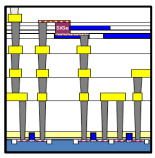
Instructor: Prof. J. Liu (Dartmouth College)

3.5 hrs

Starting proficiency: Maxwell's Equations, fiber optics technology or moderate photonics background in Group IV and III-V semiconductors

APA4

Recommended pre-requisites: APA1, APA3



Chip Process Flow for Integrated Photonics

A review of lithography and materials processing solutions for moderate to dense electronic-photonic device integration in the fabrication of a multilevel photonic integrated circuit chip. Lithography topics include areal size and density constraints for electronic versus photonic device components in one or multi-chip levels, and statistical variation of patterned structures. Materials processing topics include thermal processing history, and layout of active device components in multi-level chip design. Design challenges address multi-chip level hierarchy and power budget for an AS-PIC chip comprised of passive and active device components.

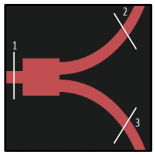
Instructor: Prof. L.C. Kimerling (MIT)

3 hrs

Starting proficiency: microelectronics or photonics background in materials processing for Group IV or III-V semiconductors

APA5

Recommended pre-requisites: APA2, APA3



Fabless Silicon Photonics Design Flow

An introduction to the Process Design Kit (PDK) methodology for design, simulation, layout, and error-check of a photonic integrated circuit. Topics covered include compact models and S-parameter theory, interpreting a PDK design guide, and circuit simulation in a design automation tool with the PDK library. Design challenges address how to layout a Mach-Zehnder modulator with the PDK component library, robust to 300mm wafer process variation, for an AS-PIC chip.

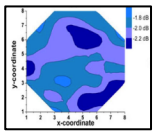
Instructor: Prof. S. Preble (RIT)

3 hrs

Starting proficiency: microelectronics or photonics background in circuit or optical link design

APA6

Recommended pre-requisites: APA2, APA4



Process Variation & Design for Manufacturing in Integrated Photonics

An introduction to process variation during fabrication of integrated photonic circuit chips, and Design for Manufacturing (DfM) solutions to ensure standardized circuit performance. Process variation topics include yield loss mechanisms (particulate defects, parametric variation), defect yield modeling, lithography and etch limitations. DfM topics include design of experiments & response surface models, corner analysis, Monte Carlo analysis, and design centering. Design challenges address how to assess sources of variation for and propose a design centered specification for a ring resonator function in an AS-PIC chip.

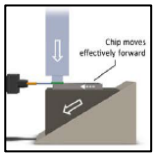
Instructor: Prof. D. Boning (MIT)

3 hrs

Starting proficiency: moderate microelectronics or photonics background in chip processing, familiarity with optically passive photonic devices

APA7

Recommended pre-requisites: APA2, APA3, APA4



Integrated Photonics Packaging

An introduction to the process requirements for photonic chip packaging and connection challenges for electrical and optical contact. Packaging process topics briefly review electronics packaging constraints (process sequence, moisture sensitivity, stress and tolerance, thermal expansion and adhesion) and their adaptation for photonics circuits. A typical packaging process is walked through along with the challenges, including optical fiber alignment and attachment for edge versus grating couplers (V-groove, passive assembly), wafer dicing, die attach and wire bonding. Design challenges address hermeticity (encapsulation) and thermal management.

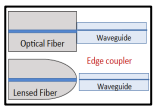
Instructor: Prof. S. Preble (RIT)

3 hrs

Starting proficiency: microelectronics or photonics background in chip processing, moderate familiarity with optically passive and active photonic devices

APA8

Recommended pre-requisites: APA1, APA2, APA3



Integrated Photonics Testing

An overview of performance criteria and characterization methods for optical, electro-optic, and opto-electronic devices in an integrated photonic circuit. Optical topics include waveguide loss measurement methods (cutback, Fabry-Perot, ring resonance), spectral characterization of resonant structures (Quality Factor, free spectral range, cavity lifetime), and Design for Test practices. Electro-optic and opto-electronic topics include RF testing of modulator speed, spectral responsivity and bandwidth measurement for detectors. Design challenges address how to evaluate an Eye diagram and assess the Bit-Error-Rate of a transceiver AS-PIC chip.

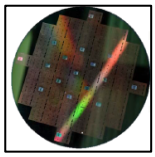
Instructor: Prof. J. Cardenas (University of Rochester)

3 hrs

Starting proficiency: introductory background in optics, familiarity with optically passive and active photonic devices

APA9

Recommended pre-requisites: APA2, APA3, APA6



Roadmapping Integrated Photonics

A review of the near term growth trends and adoption challenges for integrated photonic circuits in datacom, RF wireless, sensing, and augmented imaging applications. Topics include an overview of the Multi-Project Wafer run (MPW) process, requirements for supply-chain coordination as the integrated photonics industry proliferates into more applications, and projections for high volume production in various applications. Design challenges address identifying milestone benchmarks for an application-specific system and estimating the ramp time for high volume production of an associated AS-PIC chip.

Instructor: Prof. L.C. Kimerling (MIT)

2 hrs

Starting proficiency: moderate familiarity with optically passive and active photonic devices, familiarity with semiconductor wafer processing

Education webinar thumbnail images courtesy of participating instructors. APA2 thumbnail from RSoft Research Software. APA3 thumbnail from Proc. SPIE. **6125**, 612502 (2006). APA5 thumbnail from RSoft Research Software. APA6 thumbnail from J. Sel. Topics Q. Electr., **20**(4), July/Aug. 2014. APA7 thumbnail from 65th IEEE Electr. Comp. Tech. Conf. (ECTC) 2015, 775-782. APA9 thumbnail from AIM Photonics Institute.