

AIM Summer Academy 2019 – July 22-26, MIT Integrated Photonics: Fundamentals, Applications and Implementation PIC Fundamentals Education Track

	Monday	Tuesday	Wednesday	Thursday	Friday
Morning	8-8:50 AM	. accaay	8-8:50 PM	···a.caay	
	Registration,		Introduction to		
	Welcome	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	AIM PDK & MPW	0.00 10 17 111	0.00 // 00 ///
	S. Saini	8:30-10:20 AM	E. Timurdogan	8:30-10:45 AM	8:30-11:20 AM
	L.C. Kimerling	Integrated	L. Tilliardogan	PIC Fabrication:	Design
	9-10 AM	Photonics:	9-11:15 AM	Process Variation	Presentations
		Active Devices		and Design for	
	Photonics	J. Liu	PICs: Fabless	Manufacturing	
	Fundamentals		Silicon Photonics	D. Boning	Student Teams'
	L.C. Kimerling		Design Flow		Design Project
			S. Preble		Review
	10-12 PM				
	Integrated	10:30-12 PM	-		
	Photonics:				
	Passive Devices	Integrated			
	J.J. Hu	Photonics:		11-11:30 AM	
		Chip Process		EPDA Tool Overview	
		Flow		Mentor	
		L.C. Kimerling	11:30-12 PM	11:30-12 PM	11:30-12:30 PM
			EPDA Tool Overview	Introduction to	Conclusion
			Synopsys, Lumerical	AIM TAP Facility	- Education/Workforce
				E. White	- IPSR Roadmap
			•		L.C. Kimerling
		Lunch 12-1 PM		Group Photo	_
	Lunch 12-1 PW			Lunch 12:10-1 PM	
	1-1:30 PM	1-1:30 PM	1-2:20 PM	1-2 PM	
	EPDA Tool	EPDA Tool	Integrated	Integrated	
	Overview	Overview	Photonics	Photonics	
	Synopsys	Synopsys	Application:	Application:	
	Lumerical	Lumerical	AR Imaging	Sensing	
	1:30-2:50 PM	1:30-2:50	M. Zirngibl	B. Miller	
	Integrated	Integrated			
	Photonics	Photonics			
	Application:	Application:			
Afternoon	Datacom	Wireless	2:30-4:20 PM	2:30-4:20 PM	
	M. Glick	D. Prather	PIC Packaging	PIC	
		21110000	S. Preble	Optical & Electrical	
	3-3:30 PM	3-3:30 PM	†	Testing	
	Virtual Design	Workshop:		J. Cardenas	
	Workshop	Coventor			
	E. Verlage	M. Hargrove			
	L. Vellage	IVI. I largiove			
	3:30-6 PM	3:30-5:30 PM	1		
	Design Team	Design Team			
	Breakout Session	Breakout Session			
	Dofino Droblem	Coloot Common areas	4:30-6 PM	4:30-6:30 PM	
	Define Problem	Select Components	Design Team	Design Team	
	- Systems constraints	- Analog, Digital	Breakout Session	Breakout Session	
	- Figure of Merit				
			Plan Circuit Layout	Finalize Design	
			- Performance	- process integration	
			- Layout constraints	,	
Evening			6-8 PM		
			Networking Dinner		
			(Catalyst Restaurant /		
			Tech Square)		
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